

CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

- 1 1. A substrate adapted for use in integrated circuits, the substrate comprising:
 - 2 a first substrate layer comprising an organic material;
 - 3 a first conductor layer fabricated on an upper surface of the first substrate
 - 4 layer; and
 - 5 an integrated inductor fabricated on an upper surface of the first conductor
 - 6 layer.
- 1 2. The substrate of claim 1, wherein the integrated inductor comprises a spiral
- 2 inductor.
- 1 3. The substrate of claim 1, wherein the integrated inductor comprises a
- 2 microstrip loop inductor.
- 1 4. The substrate of claim 1, wherein the organic material is at least one of an
- 2 epoxy-based material and a liquid crystalline polymer.
- 1 5. The substrate of claim 1, further comprising a second conductor layer
- 2 fabricated on a lower surface of the first substrate layer, the second conductor layer
- 3 adapted as a ground plane for the first conductor layer.
- 1 6. The substrate of claim 1, wherein the integrated inductor and the first
- 2 conductor layer are configured in a coplanar waveguide arrangement.

1 7. The substrate of claim 1, wherein the integrated inductor comprises a cascaded
2 loop inductor comprising one or more microstrip loop inductors cascaded together.

1 8. The substrate of claim 1, further comprising a second conductor layer
2 fabricated on a lower surface of the first substrate layer, wherein two points of the
3 integrated inductor are electrically connected through a via connected to the second
4 conductor layer.

1 9. The substrate of claim 8, further comprising:
2 a second substrate layer fabricated on a lower surface of the second conductor
3 layer; and
4 a third conductor layer fabricated on a lower surface of the second substrate
5 layer.

1 10. The substrate of claim 9, wherein the second substrate layer comprises an
2 organic material.

1 11. The substrate of claim 10, wherein the organic material is at least one of an
2 epoxy-based material and a liquid crystalline polymer.

1 12. A method for fabricating a substrate adapted for use in integrated circuits, the
2 method comprising the steps of:

3 fabricating a first substrate layer comprising an organic material;

4 fabricating a first conductor layer on an upper surface of the first substrate
5 layer; and

6 fabricating an integrated inductor on an upper surface of the first conductor
7 layer.

1 13. The method of claim 12, wherein the integrated inductor comprises a spiral
2 inductor.

1 14. The method of claim 12, wherein the integrated inductor comprises a
2 microstrip loop inductor.

1 15. The method of claim 12, wherein the organic material is at least one of an
2 epoxy-based material, a liquid crystalline polymer, and a resin-coated polymer.

1 16. The method of claim 12, further comprising the step of fabricating a second
2 conductor layer on a lower surface of the first substrate layer, the second conductor
3 layer adapted as a ground plane for the first conductor layer.

1 17. The method of claim 12, wherein the steps of fabricating an integrated
2 inductor and a first conductor layer comprise fabricating the integrated inductor as a
3 coplanar waveguide inductor.

1 18. The method of claim 12, wherein the step of fabricating an integrated inductor
2 further comprises cascading one or more microstrip loop inductors together.

1 19. The method of claim 12, further comprising the step of fabricating a second
2 conductor layer on a lower surface of the first substrate layer, and wherein the step of
3 fabricating an integrated inductor comprises electrically connecting two points of the
4 integrated inductor through a via connected to the second conductor layer.

1 20. The method of claim 12, further comprising the steps of:
2 fabricating a second substrate layer on a lower surface of the second conductor
3 layer; and
4 fabricating a third conductor layer on a lower surface of the second substrate
5 layer.

1 21. The method of claim 20, wherein the second substrate layer comprises an
2 organic material.

1 22. The method of claim 21, wherein the organic material is at least one of an
2 epoxy-based material and a liquid crystalline polymer.

1 23. A substrate adapted for use in integrated circuits, the substrate comprising:
2 a first substrate layer;
3 a first conductor layer fabricated on an upper surface of the first substrate
4 layer; and
5 an integrated inductor fabricated on an upper surface of the first conductor
6 layer, the integrated inductor comprising a microstrip spiral inductor having a strip
7 width between approximately 4 mils and 40 mils and a line spacing between
8 approximately 2 mils and 4 mils.

1 24. The substrate of claim 23, wherein the first substrate layer comprises an
2 organic material.

1 25. The substrate of claim 24, wherein the organic material is at least one of an
2 epoxy-based material and a liquid crystalline polymer.

1 26. The substrate of claim 23, wherein the line width, line spacing, and number of
2 turns for the microstrip spiral inductor are configured to optimize at least one of a
3 frequency for a maximum Q factor, an effective inductance, and a self resonant
4 frequency.

1 27. The substrate of claim 23, wherein the microstrip spiral inductor comprises a
2 three-turn microstrip.

1 28. The substrate of claim 27, wherein the microstrip spiral inductor has a line
2 width of approximately 10 mils, a line spacing of approximately 2 mils, and an area of
3 approximately 4.4 millimeters².

1 29. The substrate of claim 28, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 12 nH at approximately 1.5 GHz, a maximum
3 Q factor of approximately 80 at approximately 1.5 GHz, and a self resonating
4 frequency of approximately 3.9 GHz.

1 30. The substrate of claim 27, wherein the microstrip spiral inductor has a line
2 width of approximately 7 mils, a line spacing of approximately 2 mils, and an area of
3 approximately 3.1 millimeters².

1 31. The substrate of claim 30, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 12 nH at approximately 1 GHz, a maximum Q
3 factor of approximately 100 at approximately 1 GHz, and a self resonating frequency
4 of approximately 3.2 GHz.

1 32. The substrate of claim 23, wherein the microstrip spiral inductor comprises a
2 two-turn microstrip.

1 33. The substrate of claim 32, wherein the microstrip spiral inductor has a line
2 width of approximately 10 mils, a line spacing of approximately 4 mils, and an area of
3 approximately 3.2 millimeters².

1 34. The substrate of claim 33, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 7 nH at approximately 2 GHz, a maximum Q
3 factor of approximately 100 at approximately 2 GHz, and a self resonating frequency
4 of approximately 6.8 GHz.

1 35. The substrate of claim 32, wherein the microstrip spiral inductor has a line
2 width of approximately 18 mils, a line spacing of approximately 4 mils, and an area of
3 approximately 4.5 millimeters².

1 36. The substrate of claim 35, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 5.2 nH at approximately 2 GHz, a maximum Q
3 factor of approximately 110 at approximately 2 GHz, and a self resonating frequency
4 of approximately 7 GHz.

1 37. The substrate of claim 23, wherein the microstrip spiral inductor comprises a
2 one-turn microstrip.

1 38. The substrate of claim 37, wherein the microstrip spiral inductor has a line
2 width of approximately 34 mils, a line spacing of approximately 4 mils, and an area of
3 approximately 3.2 millimeters².

1 39. The substrate of claim 38, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 1.5 nH at approximately 2.4 GHz, a maximum
3 Q factor of approximately 170 at approximately 2.4 GHz, and a self resonating
4 frequency of approximately 8.5 GHz.

1 40. A substrate adapted for use in integrated circuits, the substrate comprising:

2 a first substrate layer;

3 a first conductor layer fabricated on an upper surface of the first substrate

4 layer; and

5 an integrated inductor fabricated on an upper surface of the first conductor

6 layer, the integrated inductor comprising a coplanar waveguide loop inductor.

1 41. The substrate of claim 40, wherein the first substrate layer comprises an

2 organic material.

1 42. The substrate of claim 41, wherein the organic material is at least one of an

2 epoxy-based material and a liquid crystalline polymer.

1 43. The substrate of claim 40, wherein the number of loops comprising the

2 coplanar waveguide loop inductor is configured to optimize at least one of a frequency

3 for a maximum Q factor, an effective inductance, and a self resonant frequency.

1 44. The substrate of claim 40, wherein the coplanar waveguide loop inductor

2 comprises hollow-ground coplanar waveguide loop inductor.

1 45. A substrate adapted for use in integrated circuits, the substrate comprising:
2 a first substrate layer;
3 a first conductor layer fabricated on an upper surface of the first substrate
4 layer; and
5 an integrated inductor fabricated on an upper surface of the first conductor
6 layer, the integrated inductor comprising a microstrip loop inductor.

1 46. The substrate of claim 45, wherein the configuration of the microstrip loop
2 inductor is designed to optimize at least one of a frequency for a maximum Q factor,
3 an effective inductance, and a self resonant frequency.

1 47. The substrate of claim 45, wherein the number of loops and the line width of
2 the microstrip loop inductor are designed to optimize at least one of a frequency for a
3 maximum Q factor, an effective inductance, and a self resonant frequency.

1 48. The substrate of claim 45, wherein the microstrip loop inductor comprises a
2 single loop having a line width of approximately 2 mils and an area of approximately
3 3.5 millimeters².

1 49. The substrate of claim 48, wherein the microstrip loop inductor has an
2 effective inductance of approximately 7.7 nH, a maximum Q factor of approximately
3 90 at approximately 2.4 GHz, and a self resonating frequency of approximately 7.2
4 GHz.

1 50. The substrate of claim 45, wherein the microstrip loop inductor comprises two
2 cascaded loops.

1 51. The substrate of claim 50, wherein the microstrip loop inductor has a line
2 width of approximately 6 mils and an area of approximately 4.3 millimeters².

1 52. The substrate of claim 51, wherein the microstrip loop inductor has an
2 effective inductance of approximately 7.8 nH, a maximum Q factor of approximately
3 110 at approximately 2.1 GHz, and a self resonating frequency of approximately 6
4 GHz.

1 53. The substrate of claim 52, wherein the microstrip loop inductor has a line
2 width of approximately 4 mils and an area of approximately 3.5 millimeters².

1 54. The substrate of claim 50, wherein the microstrip loop inductor has an
2 effective inductance of approximately 10.2 nH, a maximum Q factor of approximately
3 85 at approximately 2.2 GHz, and a self resonating frequency of approximately 5
4 GHz.

1 55. The substrate of claim 45, wherein the microstrip loop inductor comprises three
2 cascaded loops.

1 56. The substrate of claim 55, wherein the microstrip loop inductor has an area of
2 approximately 4 millimeters² and a first portion of the microstrip loop inductor has a
3 line width of approximately 4 mils and a second portion of the microstrip loop
4 inductor has a line width of approximately 8 mils.

1 57. The substrate of claim 56, wherein the microstrip loop inductor has an
2 effective inductance of approximately 15 nH, a maximum Q factor of approximately
3 80 at approximately 1 GHz, and a self resonating frequency of approximately 3.2
4 GHz.

1 58. The substrate of claim 55, wherein the microstrip loop inductor has an area of
2 approximately 4 millimeters² and a first portion of the microstrip loop inductor has a
3 line width of approximately 4 mils and a second portion of the microstrip loop
4 inductor has a line width of approximately 2 mils.

1 59. The substrate of claim 58, wherein the microstrip loop inductor has an
2 effective inductance of approximately 17 nH, a maximum Q factor of approximately
3 70 at approximately 1 GHz, and a self resonating frequency of approximately 3 GHz.

1 60. A method for fabricating a substrate having integrated components and
2 adapted for use in integrated circuits, the method comprising the steps of:
3 fabricating a first substrate layer;
4 fabricating a first conductor layer on an upper surface of the first substrate
5 layer; and
6 fabricating an integrated inductor on an upper surface of the first conductor
7 layer, the integrated inductor comprising a microstrip spiral inductor having a strip
8 width between approximately 4 mils and 40 mils and a line spacing between
9 approximately 2 mils and 4 mils.

1 61. The method of claim 60, wherein the first substrate layer comprises an organic
2 material.

1 62. The method of claim 61, wherein the organic material is at least one of an
2 epoxy-based material and a liquid crystalline polymer.

1 63. The method of claim 60, wherein the step of fabricating an integrated inductor
2 further comprises configuring at least one of the line width, line spacing, and number
3 of turns for the microstrip spiral inductor to optimize at least one of a frequency for a
4 maximum Q factor, an effective inductance, and a self resonant frequency.

1 64. The method of claim 60, wherein the microstrip spiral inductor comprises a
2 three-turn microstrip.

1 65. The method of claim 64, wherein the microstrip spiral inductor has a line
2 width of approximately 10 mils, a line spacing of approximately 2 mils, and an area of
3 approximately 4.4 millimeters².

1 66. The method of claim 65, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 12 nH at approximately 1.5 GHz, a maximum
3 Q factor of approximately 80 at approximately 1.5 GHz, and a self resonating
4 frequency of approximately 3.9 GHz.

1 67. The method of claim 64, wherein the microstrip spiral inductor has a line
2 width of approximately 7 mils, a line spacing of approximately 2 mils, and an area of
3 approximately 3.1 millimeters².

1 68. The method of claim 67, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 12 nH at approximately 1 GHz, a maximum Q
3 factor of approximately 100 at approximately 1 GHz, and a self resonating frequency
4 of approximately 3.2 GHz.

1 69. The method of claim 60, wherein the microstrip spiral inductor comprises a
2 two-turn microstrip.

1 70. The method of claim 68, wherein the microstrip spiral inductor has a line
2 width of approximately 10 mils, a line spacing of approximately 4 mils, and an area of
3 approximately 3.2 millimeters².

1 71. The method of claim 70, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 7 nH at approximately 2 GHz, a maximum Q
3 factor of approximately 100 at approximately 2 GHz, and a self resonating frequency
4 of approximately 6.8 GHz.

1 72. The method of claim 69, wherein the microstrip spiral inductor has a line
2 width of approximately 18 mils, a line spacing of approximately 4 mils, and an area of
3 approximately 4.5 millimeters².

1 73. The method of claim 72, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 5.2 nH at approximately 2 GHz, a maximum Q
3 factor of approximately 110 at approximately 2 GHz, and a self resonating frequency
4 of approximately 7 GHz.

1 74. The method of claim 60, wherein the microstrip spiral inductor comprises a
2 one-turn microstrip.

1 75. The method of claim 74, wherein the microstrip spiral inductor has a line
2 width of approximately 34 mils, a line spacing of approximately 4 mils, and an area of
3 approximately 3.2 millimeters².

1 76. The method of claim 75, wherein the microstrip spiral inductor has an
2 effective inductance of approximately 1.5 nH at approximately 2.4 GHz, a maximum
3 Q factor of approximately 170 at approximately 2.4 GHz, and a self resonating
4 frequency of approximately 8.5 GHz.

1 77. A method for fabricating a substrate having integrated components and
2 adapted for use in integrated circuits, the method comprising the steps of:
3 fabricating a first substrate layer;
4 fabricating a first conductor layer on an upper surface of the first substrate
5 layer; and
6 fabricating an integrated inductor on an upper surface of the first conductor
7 layer, the integrated inductor comprising a coplanar waveguide loop inductor.

1 78. The method of claim 77, wherein the first substrate layer comprises an organic
2 material.

1 79. The method of claim 78, wherein the organic material is at least one of an
2 epoxy-based material and a liquid crystalline polymer.

1 80. The method of claim 77, wherein the step of fabricating an integrated inductor
2 further comprises configuring the number of loops of the coplanar waveguide loop
3 inductor to optimize at least one of a frequency for a maximum Q factor, an effective
4 inductance, and a self resonant frequency.

1 81. The method of claim 77, wherein the coplanar waveguide loop inductor
2 comprises a hollows-ground coplanar waveguide loop inductor.

1 82. A method for fabricating a substrate having integrated components and
2 adapted for use in integrated circuits, the method comprising the steps of:
3 fabricating a first substrate layer;
4 fabricating a first conductor layer on an upper surface of the first substrate
5 layer; and
6 fabricating an integrated inductor on an upper surface of the first conductor
7 layer, the integrated inductor comprising a microstrip loop inductor.

1 83. The method of claim 82, wherein the step of fabricating an integrated inductor
2 further comprises configuring the microstrip loop inductor to optimize at least one of
3 a frequency for a maximum Q factor, an effective inductance, and a self resonant
4 frequency.

1 84. The method of claim 82, wherein the step of fabricating an integrated inductor
2 further comprises configuring at least one of the number of loops and the line width of
3 the microstrip loop inductor to optimize at least one of a frequency for a maximum Q
4 factor, an effective inductance, and a self resonant frequency.

1 85. The method of claim 82, wherein the microstrip loop inductor comprises a
2 single loop having a line width of approximately 2 mils and an area of approximately
3 3.5 millimeters².

1 86. The method of claim 85, wherein the microstrip loop inductor has an effective
2 inductance of approximately 7.7 nH, a maximum Q factor of approximately 90 at
3 approximately 2.4 GHz, and a self resonating frequency of approximately 7.2 GHz.

1 87. The method of claim 82, wherein the microstrip loop inductor comprises two
2 cascaded loops.

1 88. The method of claim 87, wherein the microstrip loop inductor has a line width
2 of approximately 6 mils and an area of approximately 4.3 millimeters².

1 89. The method of claim 88, wherein the microstrip loop inductor has an effective
2 inductance of approximately 7.8 nH, a maximum Q factor of approximately 110 at
3 approximately 2.1 GHz, and a self resonating frequency of approximately 6 GHz.

1 90. The method of claim 87, wherein the microstrip loop inductor has a line width
2 of approximately 4 mils and an area of approximately 3.5 millimeters².

1 91. The method of claim 90, wherein the microstrip loop inductor has an effective
2 inductance of approximately 10.2 nH, a maximum Q factor of approximately 85 at
3 approximately 2.2 GHz, and a self resonating frequency of approximately 5 GHz.

1 92. The method of claim 82, wherein the microstrip loop inductor comprises three
2 cascaded loops.

1 93. The method of claim 92, wherein the microstrip loop inductor has an area of
2 approximately 4 millimeters² and a first portion of the microstrip loop inductor has a
3 line width of approximately 4 mils and a second portion of the microstrip loop
4 inductor has a line width of approximately 8 mils.

1 94. The method of claim 93, wherein the microstrip loop inductor has an effective
2 inductance of approximately 15 nH, a maximum Q factor of approximately 80 at
3 approximately 1 GHz, and a self resonating frequency of approximately 3.2 GHz.

1 95. The method of claim 92, wherein the microstrip loop inductor has an area of
2 approximately 4 millimeters² and a first portion of the microstrip loop inductor has a
3 line width of approximately 4 mils and a second portion of the microstrip loop
4 inductor has a line width of approximately 2 mils.

1 96. The method of claim 95, wherein the microstrip loop inductor has an effective
2 inductance of approximately 17 nH, a maximum Q factor of approximately 70 at
3 approximately 1 GHz, and a self resonating frequency of approximately 3 GHz.

1 97. A computer program embodied in a computer-readable medium for optimizing
2 the design of an integrated inductor in a substrate adapted for use in integrated
3 circuits, the computer program comprising:

4 logic configured to receive one or more design parameters for a substrate
5 structure in which an inductor is to be integrated, the design parameters specifying at
6 least one of the material characteristics, the physical characteristics, and electrical
7 characteristics of one or more substrate layers and one or more conductor layers
8 comprising the substrate structure;

9 logic configured to receive one or more process parameters associated with a
10 predetermined type of integrated circuit package in which the substrate structure is to
11 be implemented;

12 logic configured to generate a coupled-line model for a plurality of
13 configurations for an integrated inductor, the coupled-line model comprising one or
14 more coupled lines and one or more discontinuities;

15 logic configured to simulate the frequency response of the coupled-line models
16 based on the design parameters and process parameters; and
17 logic configured to determine an optimal configuration for the integrated inductor
18 which satisfies the design parameters and process parameters.

1 98. The computer program of claim 101, further comprising logic configured to
2 provide the optimal layout for an integrated inductor.

1 99. The computer program of claim 97, wherein the logic configured to simulate
 2 the frequency response comprises:

3 segmenting the coupled-line model of the integrated inductor into individual
 4 segments;

5 calculating an impedance matrix for each of the segments in the coupled-line
 6 model; and

7 determining the frequency response of the combination of the segments.

1 100. The computer program of claim 99, wherein the logic configured to simulate
 2 the frequency response further comprises solving the following system of equations
 3 for each of a set of pairs of symmetric lossless coupled lines:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix};$$

5 wherein:

6 V_1 = voltage at a first node of a first lossless coupled line;
 7 V_2 = voltage at a first node of a second lossless coupled
 8 line;
 9 V_3 = voltage at a second node of the first lossless coupled
 10 line;
 11 V_4 = voltage at a second node of the second lossless
 12 coupled line;
 13 l = length of coupled lines;
 14 Z_{oe} = even-mode impedance;
 15 Z_{oo} = odd-mode impedance;
 16 β_e = even-mode propagation constant;
 17 β_o = odd-mode propagation constant;

$$\begin{aligned} Z_{11} &= Z_{22} = Z_{33} = Z_{44} = -j(Z_{oe} \cot(\beta_e l) + Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{12} &= Z_{21} = Z_{34} = Z_{43} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{13} &= Z_{24} = Z_{31} = Z_{42} = -j(Z_{oe} \csc(\beta_e l) + Z_{oo} \csc(\beta_o l)) / 2 \\ Z_{14} &= Z_{23} = Z_{32} = Z_{41} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \csc(\beta_o l)) / 2 \end{aligned}$$

1 101. The computer program of claim 97, wherein the logic configured to generate a
2 coupled-line model is adapted to model at least one of a coplanar waveguide loop
3 inductor, a microstrip loop inductor, and a microstrip spiral inductor.

1 102. The computer program of claim 97, wherein the logic configured to receive
2 one or more design parameters for a substrate structure is further configured to receive
3 one or more design parameters for the integrated inductor to be designed.

1 103. The computer program of claim 102, wherein the one or more design
2 parameters for the integrated inductor specifies a type of integrated inductor to be
3 designed.

1 104. The computer program of claim 103, wherein the type of integrated inductor
2 comprises one of a coplanar waveguide loop inductor, a microstrip loop inductor, and
3 a microstrip spiral inductor.

1 105. The computer program of claim 102, wherein the one or more design
2 parameters for the integrated inductor comprises at least one of a predetermined line
3 width for the integrated inductor, a predetermined line spacing for the integrated
4 inductor, a predetermined maximum area for the integrated inductor, a predetermined
5 inductance value for the integrated inductor, a predetermined frequency, a
6 predetermined minimum Q factor for the integrated inductor, and a predetermined self
7 resonant frequency for the integrated inductor.

1 106. A system for optimizing the design of an integrated inductor in a substrate
2 adapted for use in integrated circuits, the system comprising:
3 means for receiving one or more design parameters for a substrate structure in
4 which an inductor is to be integrated and one or more process parameters associated
5 with a predetermined type of integrated circuit package in which the substrate
6 structure is to be implemented, the design parameters specifying at least one of the
7 material characteristics, the physical characteristics, and electrical characteristics of
8 one or more substrate layers and one or more conductor layers comprising the
9 substrate structure;
10 means for generating a coupled-line model for a plurality of configurations for
11 an integrated inductor, the coupled-line model comprising one or more coupled lines
12 and one or more discontinuities;
13 means for simulating the frequency response of the coupled-line models based
14 on the design parameters and process parameters; and
15 means for determining an optimal configuration for the integrated inductor which
16 satisfies the design parameters and process parameters.

1 107. The system of claim 106, further comprising a means for providing the optimal
2 layout for an integrated inductor.

1 108. The system of claim 106, wherein means for simulating comprises:

2 means for segmenting the coupled-line model of the integrated inductor into

3 individual segments;

4 means for calculating an impedance matrix for each of the segments in the

5 coupled-line model; and

6 means for determining the frequency response of the combination of the

7 segments.

1 109. The system of claim 108, wherein the means for simulating further comprises

2 a means for solving the following system of equations for each of a set of pairs of

3 symmetric lossless coupled lines:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix};$$

5 wherein:

6 V_1 = voltage at a first node of a first lossless coupled line;

7 V_2 = voltage at a first node of a second lossless coupled

8 line;

9 V_3 = voltage at a second node of the first lossless coupled

10 line;

11 V_4 = voltage at a second node of the second lossless

12 coupled line;

13 l = length of coupled lines;

14 Z_{oe} = even-mode impedance;

15 Z_{oo} = odd-mode impedance;

16 β_e = even-mode propagation constant;

17 β_o = odd-mode propagation constant;

$$\begin{aligned} Z_{11} &= Z_{22} = Z_{33} = Z_{44} = -j(Z_{oe} \cot(\beta_e l) + Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{12} &= Z_{21} = Z_{34} = Z_{43} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{13} &= Z_{24} = Z_{31} = Z_{42} = -j(Z_{oe} \csc(\beta_e l) + Z_{oo} \csc(\beta_o l)) / 2 \\ Z_{14} &= Z_{23} = Z_{32} = Z_{41} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \csc(\beta_o l)) / 2 \end{aligned}$$

1 110. The system of claim 106, wherein the means for generating a coupled-line
2 model is adapted to model at least one of a coplanar waveguide loop inductor, a
3 microstrip loop inductor, and a microstrip spiral inductor.

1 111. The system of claim 106, wherein the means for receiving further receives one
2 or more design parameters for the integrated inductor to be designed.

1 112. The system of claim 106, wherein the one or more design parameters for the
2 integrated inductor specify a type of integrated inductor to be designed.

1 113. The system of claim 112, wherein the type of integrated inductor comprises
2 one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a
3 microstrip spiral inductor.

1 114. The computer program of claim 111, wherein the one or more design
2 parameters for the integrated inductor comprises at least one of a predetermined line
3 width for the integrated inductor, a predetermined line spacing for the integrated
4 inductor, a predetermined maximum area for the integrated inductor, a predetermined
5 inductance value for the integrated inductor, a predetermined frequency, a
6 predetermined minimum Q factor for the integrated inductor, and a predetermined self
7 resonant frequency for the integrated inductor.

1 115. A system for optimizing the design of an integrated inductor in a substrate
2 adapted for use in integrated circuits, the system comprising:
3 logic configured to receive one or more design parameters for a substrate
4 structure in which an inductor is to be integrated, the design parameters specifying at
5 least one of the material characteristics, the physical characteristics, and electrical
6 characteristics of one or more substrate layers and one or more conductor layers
7 comprising the substrate structure;
8 logic configured to receive one or more process parameters associated with a
9 predetermined type of integrated circuit package in which the substrate structure is to
10 be implemented;
11 logic configured to generate a coupled-line model for a plurality of
12 configurations for an integrated inductor, the coupled-line model comprising one or
13 more coupled lines and one or more discontinuities;
14 logic configured to simulate the frequency response of the coupled-line models
15 based on the design parameters and process parameters;
16 logic configured to determine an optimal configuration for the integrated
17 inductor which satisfies the design parameters and process parameters; and
18 a processing device configured to implement the logic.

1 116. The system of claim 115, further comprising a user interface device configured
2 to enable a user to input the design parameters and the process parameters.

1 117. The system of claim 115, further comprising logic configured to provide the
2 optimal layout for an integrated inductor.

1 118. The system of claim 117, further comprising a display device configured to
2 display the optimal layout.

1 119. The system of claim 115, wherein the logic configured to simulate the
2 frequency response comprises:

3 segmenting the coupled-line model of the integrated inductor into individual

4 segments;

5 calculating an impedance matrix for each of the segments in the coupled-line
6 model; and

7 determining the frequency response of the combination of the segments.

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1 120. The system of claim 115, wherein the logic configured to simulate the
 2 frequency response further comprises solving the following system of equations for
 3 each of a set of pairs of symmetric lossless coupled lines:

4

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix};$$

5 wherein:

6 V_1 = voltage at a first node of a first lossless coupled line;
 7 V_2 = voltage at a first node of a second lossless coupled
 8 line;
 9 V_3 = voltage at a second node of the first lossless coupled
 10 line;
 11 V_4 = voltage at a second node of the second lossless
 12 coupled line;
 13 l = length of coupled lines;
 14 Z_{oe} = even-mode impedance;
 15 Z_{oo} = odd-mode impedance;
 16 β_e = even-mode propagation constant;
 17 β_o = odd-mode propagation constant;

19

$$\begin{aligned} Z_{11} &= Z_{22} = Z_{33} = Z_{44} = -j(Z_{oe} \cot(\beta_e l) + Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{12} &= Z_{21} = Z_{34} = Z_{43} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \cot(\beta_o l)) / 2 \\ Z_{13} &= Z_{24} = Z_{31} = Z_{42} = -j(Z_{oe} \csc(\beta_e l) + Z_{oo} \csc(\beta_o l)) / 2 \\ Z_{14} &= Z_{23} = Z_{32} = Z_{41} = -j(Z_{oe} \cot(\beta_e l) - Z_{oo} \csc(\beta_o l)) / 2 \end{aligned}$$

1 121. The system of claim 115, wherein the logic configured to generate a coupled-
 2 line model is adapted to model at least one of a coplanar waveguide loop inductor, a
 3 microstrip loop inductor, and a microstrip spiral inductor.

1 122. The system of claim 115, wherein the logic configured to receive one or more
 2 design parameters for a substrate structure is further configured to receive one or more
 3 design parameters for the integrated inductor to be designed.

1 123. The system of claim 122, wherein the one or more design parameters for the
2 integrated inductor specifies a type of integrated inductor to be designed.

1 124. The system of claim 123, wherein the type of integrated inductor comprises
2 one of a coplanar waveguide loop inductor, a microstrip loop inductor, and a
3 microstrip spiral inductor.

1 125. The system of claim 122, wherein the one or more design parameters for the
2 integrated inductor comprises at least one of a predetermined line width for the
3 integrated inductor, a predetermined line spacing for the integrated inductor, a
4 predetermined maximum area for the integrated inductor, a predetermined inductance
5 value for the integrated inductor, a predetermined frequency, a predetermined
6 minimum Q factor for the integrated inductor, and a predetermined self resonant
7 frequency for the integrated inductor.

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